2.5V / 3.3V PHASE-LOCK LOOP CLOCK DRIVER ZERO DELAY BUFFER

IDT5V2528/A

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES OCTOBER 28, 2014

FEATURES:

- **Operates at 3.3V V_{DD}/AV_{DD} and 2.5V/3.3V V_{DDQ}**
- **1:10 fanout**
- **3-level inputs for output control**
- **External feedback (FBIN) pin is used to synchronize the outputs to the clock input signal**
- **No external RC network required for PLL loop stability**
- **Configurable 2.5V or 3.3V LVTTL outputs**
- **t_{PD} Phase Error at 100MHz to 166MHz: ±150ps**
- **Jitter (peak-to-peak) at 133MHz and 166MHz: ±75ps**
- **Spread spectrum compatible**
- **Operating Frequency:**
  - **Std: 25MHz to 140MHz**
  - **A: 25MHz to 167MHz**
- **Available in TSSOP package**
- **Use replacement part 87952AYI-147LF**

DESCRIPTION:

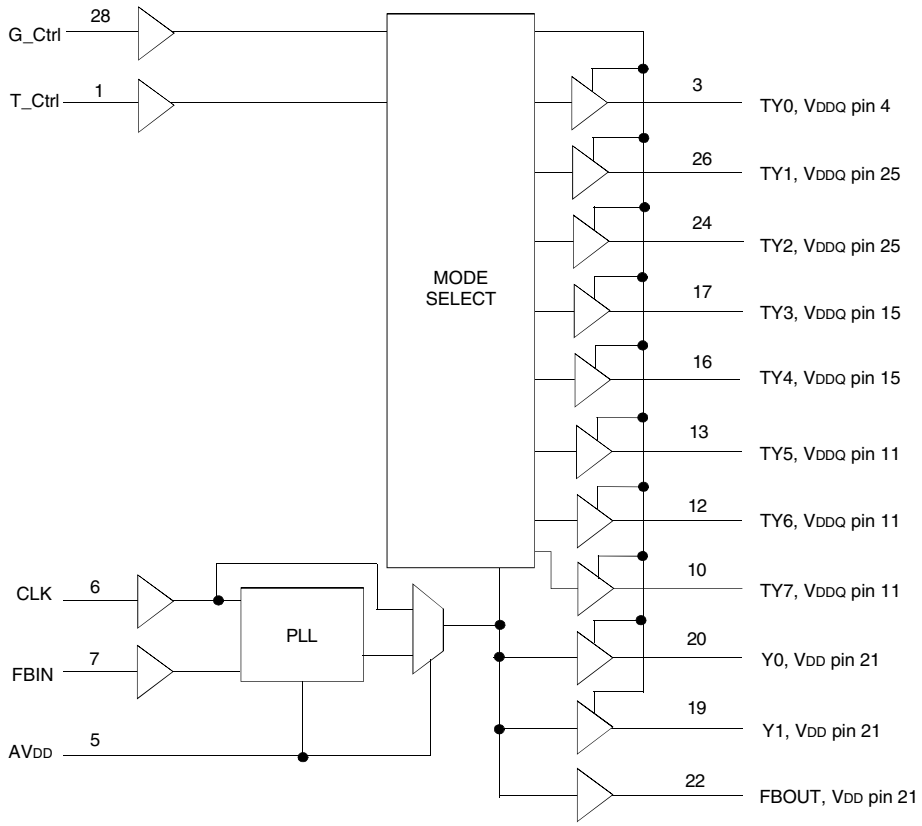
The IDT5V2528 is a high performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. The IDT5V2528 inputs, PLL core, Y0, Y1, and FB_{OUT} buffers operate from the 3.3V V_{DD} and AV_{DD} power supply pins.

One bank of ten outputs provide low-skew, low-jitter copies of CLK. Of the ten outputs, up to seven may be configured for 2.5V or 3.3V LVTTL outputs. The number of 2.5V outputs is controlled by 3-level input signals G_Ctrl and T_Ctrl, and by connecting the appropriate V_{DDQ} pins to 2.5V or 3.3V. The 3-level input signals may be hard-wired to high-mid-low levels. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLK. The outputs can be enabled or disabled via the G_Ctrl input. When the G_Ctrl input is mid or high, the outputs switch in phase and frequency with CLK; when the G_Ctrl is low, all outputs (except FB_{OUT}) are disabled to the logic-low state.

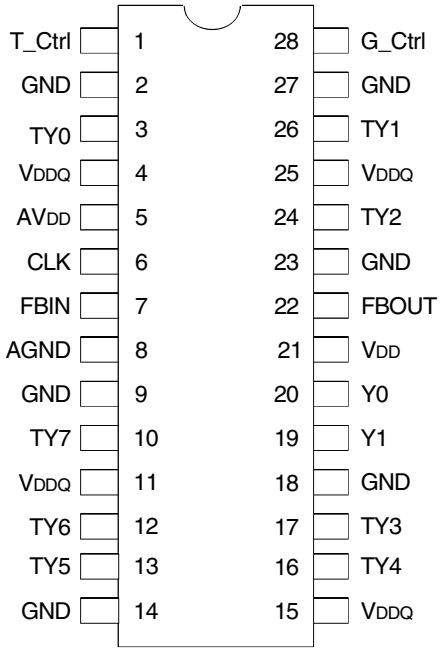
Unlike many products containing PLLs, the IDT5V2528 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the IDT5V2528 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by strapping AVDD to ground.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max.	Unit
V_{DD}, V_{DDQ}, AV_{DD}	Supply Voltage Range	–0.5 to +4.6	V
V_I(2)	Input Voltage Range	–0.5 to +5.5	V
V_O(2)	Voltage Range applied to any output in the HIGH or LOW state	–0.5 to V_{DD}+0.5	V
I_{IK} (V_I < 0)	Input Clamp Current	–50	mA
I_{OK} (V_O < 0 or V_O > V_{DD})	Output Clamp Current	±50	mA
I_O (V_O = 0 to V_{DD})	Continuous Output Current	±50	mA
V_{DD} or GND	Continuous Current	±200	mA
T_{STG}	Storage Temperature Range	–65 to +150	°C
T_J	Junction Temperature	+150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

CAPACITANCE(1)

Symbol	Description		Min	Typ.	Max.	Unit
C_{IN}	Input Capacitance V_I = V_{DD} or GND		—	5	—	pF
C_O	Output Capacitance V_I = V_{DD} or GND		—	6	—	pF
C_L	Load Capacitance	2.5V outputs	—	20	—	pF
		3.3V outputs	—	30	—	

NOTE:
1. Unused inputs must be held HIGH or LOW to prevent them from floating.

RECOMMENDED OPERATING RANGE

Symbol	Description		Min.	Typ.	Max.	Unit
V_{DD}, AV_{DD}(1)	Power Supply Voltage		3	3.3	3.6	V
V_{DDQ}(1)	Power Supply Voltage	2.5V Outputs	2.3	2.5	2.7	V
		3.3V Outputs	3	3.3	3.6	
T_A	Ambient Operating Temperature		–40	+25	+85	°C

NOTE:
1. All power supplies should operate in tandem. If V_{DD} or V_{DDQ} is at a maximum, then V_{DDQ} or V_{DD} (respectively) should be at maximum, and vice-versa.

PIN DESCRIPTION

Terminal			
Name	**No.**	**Type**	**Description**
CLK(1)	6	I	Clock input
FBIN	7	I	Feedback input
G_Ctrl(2)	28	3-level	3-level input for 2.5V / 3.3V Output Select/ Output bank enable. When G_Ctrl is LOW, all outputs except FBOUT are disabled to a logic-LOW state. When G_Ctrl is MID or HIGH, all outputs are enabled and switch at the same frequency as CLK (see OUTPUT SELECTION table).
T_Ctrl(2)	1	3-level	3-level input for 2.5V / 3.3V Output Select (see OUTPUT SELECTION table)
FBOUT	22	O	Feedback output
TY(7:0)	3, 10, 12, 13, 16, 17, 24, 26	O	2.5V or 3.3V Clock outputs. 1, 2, 3, 5, or 7 of these outputs may be selected as 2.5V outputs (see OUTPUT SELECTION table).
Y(1:0)	19, 20	O	3.3V Clock Outputs
AV_{DD}(3)	5	Power	3.3V Analog power supply. AV_{DD} provides the power reference for the analog circuitry.
AGND	8	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V_{DD}	21	Power	3.3V Power supply
V_{DDQ}	4, 11, 15, 25	Power	2.5V or 3.3V Power supply for TY outputs
GND	2, 9, 14, 18 23, 27	Ground	Ground

NOTES:
1. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time of 1ms is required for the PLL to phase lock the feedback signal to the reference signal.
2. 3-level inputs will float to MID logic level if left unconnected.
3. AV_{DD} can be used to bypass the PLL for test purposes. When AV_{DD} is strapped to ground, PLL is bypassed and CLK is buffered directly to the outputs.

STATIC FUNCTION TABLE (AV_{DD} = 0V)(1)

Inputs			Outputs		
G_Ctrl	**T_Ctrl**	**CLK**	**TY(7:0)**	**Y(1:0)**	**FBOUT**
L	X	L	L	L	L
L	X	H	L	L	H
see OUTPUT SELECTION table		H	H	H	H
		L	L	L	L
		running	running	running	running

NOTE:
1. AV_{DD} should be powered up along with V_{DD}, before setting AV_{DD} to ground, to put the control pins in a valid state.

OUTPUT SELECTION

G_Ctrl	T_Ctrl	TY(7:0)	V_{DDQ} Configuration
M	L	TY_0 (2.5V) TY_1 - TY_7 (3.3V)	Pin 4 (2.5V) Pins 11, 15, 25 (3.3V)
M	M	TY_1, TY_2 (2.5V) TY_0, TY_3 - TY_7 (3.3V)	Pin 25 (2.5V) Pins 4, 11, 15 (3.3V)
M	H	TY_0 - TY_2 (2.5V) TY_3 - TY_7 (3.3V)	Pins 4, 25 (2.5V) Pins 11, 15 (3.3V)
H	L	TY_0 - TY_4 (2.5V) TY_5 - TY_7 (3.3V)	Pins 4, 15, 25 (2.5V) Pin 11 (3.3V)
H	M	TY_1 - TY_7 (2.5V) TY_0 (3.3V)	Pins 11, 15, 25 (2.5V) Pin 4 (3.3V)
H	H	TY_0 - TY_7 (3.3V)	Pins 4, 11, 15, 25 (3.3V)

DYNAMIC FUNCTION TABLE (AV_{DD} = 3.3V)

Inputs			Outputs		
G_Ctrl	**T_Ctrl**	**CLK**	**TY(7:0)**	**Y(1:0)**	**FBOUT**
L	X	L	L	L	L
L	X	H	L	L	H
see OUTPUT SELECTION table		L	L	L	L
		H	H	H	H

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max	Unit
V_{IK}	Input Clamp Voltage	I_I = -18mA				- 1.2	V
V_{IH}	Input HIGH Level	CLK, FBIN		2			V
V_{IL}	Input LOW Level	CLK, FBIN				0.8	V
V_{IHH}	Input HIGH Voltage Level(2)	3-Level Inputs Only		V_{DD} - 0.6			V
V_{IMM}	Input MID Voltage Level(2)	3-Level Inputs Only		V_{DD}/2 - 0.3		V_{DD}/2 + 0.3	V
V_{ILL}	Input LOW Voltage Level(2)	3-Level Inputs Only				0.6	V
V_{OH}	Output HIGH Voltage Level (3.3V Outputs)	I_{OH} = -100µA		V_{DD} - 0.2			V
		I_{OH} = -12mA		2.4			
V_{OH}	Output HIGH Voltage Level (2.5V Outputs)	I_{OH} = -100µA		V_{DD} - 0.1			V
		I_{OH} = -12mA		2			
V_{OL}	Output LOW Voltage Level (3.3V Outputs)	I_{OL} = 100µA				0.2	V
		I_{OL} = 12mA				0.4	
V_{OL}	Output LOW Voltage Level (2.5V Outputs)	I_{OL} = 100µA				0.1	V
		I_{OL} = 12mA				0.4	
I_{3}	3-Level Input DC Current (G_Ctrl, T_Ctrl)	V_{IN} = V_{DD}	HIGH Level			+200	µA
		V_{IN} = V_{DD}/2	MID Level	–50		+50	
		V_{IN} = GND	LOW Level	–200			
I_I	Input Current	V_I = V_{DD} or GND				±5	µA

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.
2. These inputs are normally wired to V_{DD}, GND, or left floating. Internal termination resistors bias floating inputs to V_{DD}/2. If these inputs are switched, the function and timing of the outputs may be glitched, and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions	Typ.(1)	Max	Unit
I_{DDPD}	Power Down Supply Current	V_{DD} = 3.6, V_{DDQ} = 2.7V / 3.3V, AV_{DD} = 0V	8	40	µA
I_{DDA}	AV_{DD} Supply Current	V_{DD} = AV_{DD} = 3.6V, V_{DDQ} = 2.7V / 3.3V, CLK = 0 or V_{DD}	3.5	10	mA
I_{DD}	Dynamic Power Supply Current	V_{DD} = AV_{DD} = 3.6V, V_{DDQ} = 2.7V / 3.3V, C_L = 0pF	500	—	µA/MHz
I_{DDD}	Dynamic Power Supply Current per Output	V_{DD} = AV_{DD} = V_{DDQ} = 3.6V C_L = 30pF, CLK = 100MHz	15	—	mA
		V_{DD} = AV_{DD} = 3.6V, V_{DDQ} = 2.7V C_L = 20pF, CLK = 100MHz	12	—	

NOTE:

1. For nominal voltage and temperature.

INPUT TIMING REQUIREMENTS OVER OPERATING RANGE

		5V2528		5V2528A		Units
		Min	Max	Min	Max	
f_{CLOCK}	Clock frequency	25	140	25	167	MHz
	Input clock duty cycle	40%	60%	40%	60%	
t_{LOCK}	Stabilization time(1)		1		1	ms

NOTE:
1.Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - 5V2528(1)

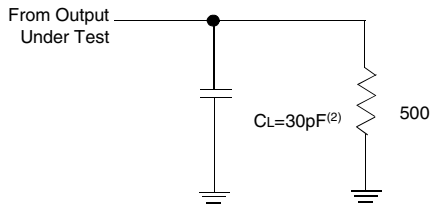
Symbol	Parameter(2)	Min.	Typ.	Max.	Unit
t_{PHASE} error	Phase Error from Rising Edge CLK to Rising Edge FBIN (100MHz-133MHz)	–150	—	150	ps
t_{PHASE} error - jitter(3)	Phase Error minus Jitter from Rising Edge CLK to Rising Edge FBIN (133MHz)	–50	—	50	ps
$t_{SK1(0)}$(4)	Output Skew between 3.3V Outputs	—	—	150	ps
$t_{SK2(0)}$(4)	Output Skew between 2.5V Outputs	—	—	150	ps
$t_{SK3(0)}$(4,5)	Output Skew between 2.5V and 3.3V Outputs	—	—	200	ps
t_J	Cycle-to-Cycle Output Jitter (Peak-to-Peak) at 133MHz	–75	—	75	ps
	Duty Cycle	45	—	55	%
t_R	Output Rise Time for 3.3V Outputs (20% to 80%)	0.8	—	2.1	ns
t_F	Output Fall Time for 3.3V Outputs (20% to 80%)	0.8	—	2.1	ns
t_R	Output Rise Time for 2.5V Outputs (20% to 80%)	0.5	—	1.5	ns
t_F	Output Fall Time for 2.5V Outputs (20% to 80%)	0.5	—	1.5	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - 5V2528A(1)

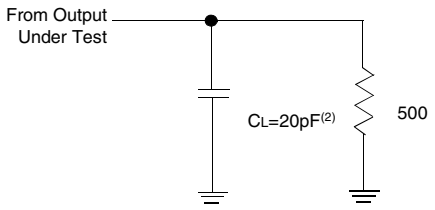
Symbol	Parameter(2)		Min.	Typ.	Max.	Unit
t_{PHASE} error	Phase Error from Rising Edge CLK to Rising Edge FBIN (100MHz-166MHz)		–150	—	150	ps
t_{PHASE} error - jitter(3)	Phase Error minus Jitter from Rising Edge CLK to Rising Edge FBIN (166MHz)		–50	—	50	ps
$t_{SK1(0)}$(4)	Output Skew between 3.3V Outputs		—	—	150	ps
$t_{SK2(0)}$(4)	Output Skew between 2.5V Outputs		—	—	150	ps
$t_{SK3(0)}$(4,5)	Output Skew between 2.5V and 3.3V Outputs	25MHz to 133MHz	—	—	200	ps
		133MHz to 166MHz	—	—	250	
t_J	Cycle-to-Cycle Output Jitter (Peak-to-Peak) at 166MHz		–75	—	75	ps
	Duty Cycle		45	—	55	%
t_R	Output Rise Time for 3.3V Outputs (20% to 80%)		0.8	—	2.1	ns
t_F	Output Fall Time for 3.3V Outputs (20% to 80%)		0.8	—	2.1	ns
t_R	Output Rise Time for 2.5V Outputs (20% to 80%)		0.5	—	1.5	ns
t_F	Output Fall Time for 2.5V Outputs (20% to 80%)		0.5	—	1.5	ns

NOTES:
1. All parameters are measured with the following load conditions: 30pF || 500Ω for 3.3V outputs and 20pF || 500Ω for 2.5V outputs.
2. The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.
3. Phase error does not include jitter.
4. All skew parameters are only valid for equal loading of all outputs.
5. Measured for V_{DDQ} = 2.3V and 3V, 2.5V and 3.3V, or 2.7V and 3.6V.

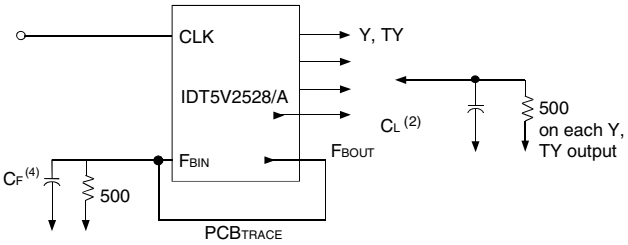
TEST CIRCUIT AND VOLTAGE WAVEFORMS

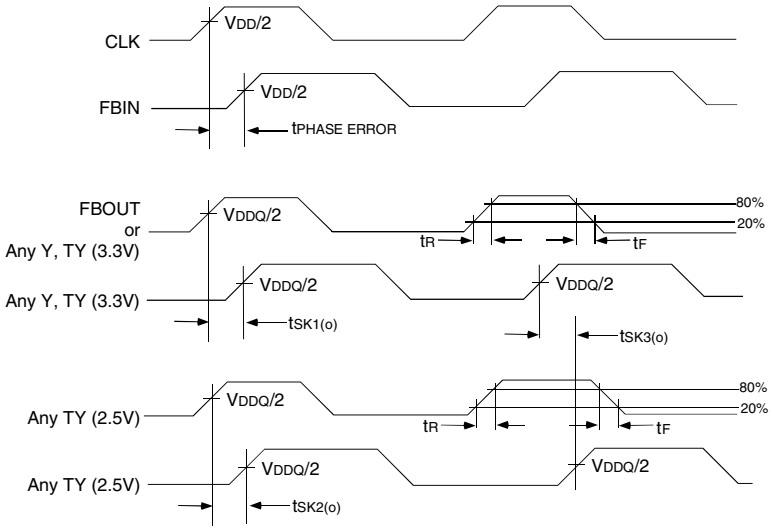


Test Circuit for 3.3V Outputs



Test Circuit for 2.5V Outputs



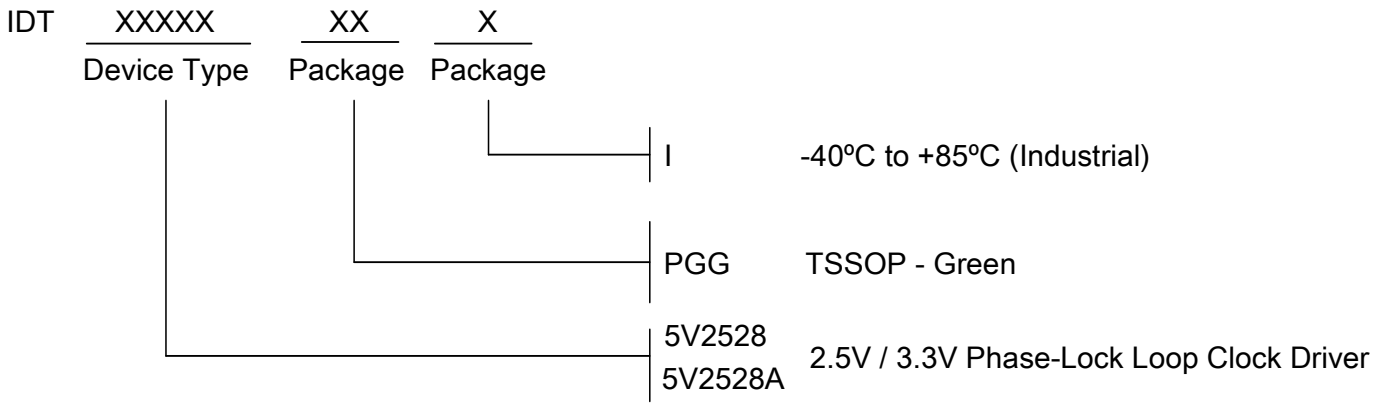


PHASE ERROR AND SKEW CALCULATIONS(3,4)

NOTES:

1. All inputs pulses are supplied by generators having the following characteristics: PRR ≤ 100MHz ZO = 50Ω, tR ≤ 1.2 ns, tF ≤ 1.2 ns.
2. CL includes probe and jig capacitance.
3. The outputs are measured one at a time with one transition per measurement.
4. Phase error measurements require equal loading at outputs Y, TY, and FBOUT. CF = CL – CFBIN – CPCBtrace; CFBIN ≅ 5pF.

ORDERING INFORMATION



REVISION HISTORY

Rev	Table	Page	Discription of Change	Date
A		1	NRND - Not Recommended for New Designs	5/16/13
A		1	Product Discontinuation Notice - Last Time Buy Expires on October 28, 2014, PDN# CQ-13-02	12/3/13

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